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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PADGETT, MARIANNE L	

ART UNIT	PAPER NUMBER
1792	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/674,647	CHOE ET AL.	
	Examiner	Art Unit	
	MARIANNE L. PADGETT	1792	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 June 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *26-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *26-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. Applicants' 6/1/2009 amendment to the specification which removes the changes made in the 11/24/2008 amendment, hence removes the new matter inserted thereby, overcomes the objection to the specification made in section 3 of the 3/17/2009 action.

Applicants have canceled all previous claims, providing a new set of claims containing 3 independent claims, which have overlapping issues with the previously examined claims, but are of different scope therefrom, as well as having different scopes and issues from the original claims, therefore require new review of both support & other formalities, as well as prior art. New 112 problems, both first & second, introduced by applicant's new set of claims are discussed below.

With respect to **Bendernagel et al**. (6,800,518 B2), the examiner agrees that the process as disclosed therein, while making composites having buried insulated layers made by analogous processing steps to those taught by applicants (parts thereof claimed) & while also creating void structures in combination with the SOI (silicon-on-insulator) structures, only provides teachings for making the void structures & buried insulating regions adjacent to each other, including wherein multilayers of such composite structures are made. In column 8, line 63-column 9, line 20, especially 8-10 state in "buried oxide/void formation, the porous Si is consumed and the epi-Si layer may be thinned by surface oxidation, resulting in a much thinner Si overlayer..." which would appear to indicate that all of the porous layer is changed to either buried oxide or void formation (i.e. a different porous structure), with no indication of any void formation beneath the oxide formation. For these reasons, **Bendernagel et al**. (518) does not read all the new claims.

2. With respect to meanings & terms defined by the specification, it is again noted that [0026] defines "**Si-containing**" as denoting "a semiconductor material that includes at least silicon" providing nonlimiting examples of Si, SiGe, SiC, SiGeC, epi-Si/Si, etc., hence while most people reading the claims would assume that "a Si-containing substrate" as claimed includes glass or silicon dioxide, etc., in light of the specification's definition this limitation actually requires the substrate to either be a Si-

containing semiconductor material, or for a portion of it, such as a layer to be a Si-containing semiconductor material. Note that as claimed, the substrate may be a composite substrate & the silicon containing portion may be anywhere in the composite substrate, i.e. need not be on the surface or exposed in any fashion, nor need it be a continuous layer, etc. Note that as "Si-containing" & "silicon containing" are literally identical meanings, they are both considered to be bound by the definition of [0026].

The preambles of all the independent claims introduced the limitation of "uniform buried oxide layer" or "uniform buried oxide region", were also as previously noted [0012] defines "**uniform**" as denoting "a buried oxide **region** having a **continuous interface** with the Si-containing **overlayer** as well as the **underlying Si-containing substrate** wherein the variation of thickness **across the entire wafer** is less than 30 % of the total thickness of the buried oxide layer" (emphasis added), such that this otherwise relative term has a very specific meaning which is only applicable to the buried oxide layer. The examiner further notes that while the last four lines of **claim 26** contain the definition from [0012] (which is desirable, because it does provide more easily recognized and understood meaning), both of independent **claims 31 & 36** positively recite formation of "uniform buried oxide region", hence in light of the specification also are necessarily limited by this definition.

With respect to the "voids" in claims 26-27, 31-32 & 36, the examiner notes that a void may simply be a pore that has been sealed or closed off from the surface. The formation avoids is discussed in [0043], where figures 2E-2H provide illustrations of a uniform buried oxide layer, or plural buried oxide regions with voids thereunder in a remaining porous region 12, thus supporting the claimed location of voids under a single uniform buried oxide layer, or under a patterned layer with plural buried oxide regions. As claimed size of voids formed are not limited, nor are number of voids, as long as there are plural (i.e. more than one).

3. **Claims 26-42** are rejected under 35 U.S.C. **112, second** paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In all three independent **claims 26, 31 & 36**, applicants have introduced "a Si-containing **substrate**" (emphasis added) in lines 4, where the first two listed "forming..." limitations have a clear relationship to each other, however the third "forming... into **said wafer**" (emphasis added) has no clear relationship to the preceding limitations, since "said wafer" has absolutely no antecedent basis or any relationship thereto due to the use of completely different word choice, thus unrelated nomenclature, hence the claim process is vague, indefinite and unclear, since as written it becomes unclear whether to different workpieces (e.g. the claimed substrate & the claimed wafer) are being treated in the process & what their relationship, if any, should be, or if they should be treated as the same workpiece.

In **claims 26, 31 & 36**, the third "forming" limitations have the limitation of "wherein **the** oxygen peak is located...", (emphasis added) however "the oxygen peak" lacks any antecedent basis, plus lacks clear context to give it a clear meaning, as a "peak" may be the apex physical structure or the apex of data on a graph, or the like. The examiner notes that this is the same language as is employed in [0037], although implanting ions, instead of implanting atoms that need not be ions, however this paragraph having more detail may be considered to have sufficient context to provide clarifying language to the claims for applicants' probable intent. If one was implanting oxygen ions (not necessitated by the claims), instead of atoms, applicants **may be** able to provide arguments on why the claim language could be clarified to say something like -- wherein a peak oxygen amount [or concentration] of oxygen from the oxygen ion implanting, it is located... -- with reference to how such jargon (oxygen peak) is generally interpreted in the field of ion implantation, however since no ion implantation is necessary, no such arguments could presently be made.

In **claim 26**, lines 13-14 state "wherein **said** porous silicon containing **region** includes voids that are located beneath said uniform buried oxide layer after said annealing" (emphasis added), which limitation is extremely confusing as written, since antecedence says that said region is that which was formed in the initial forming step of lines 3-4, however this limitation at requires it to be underneath the buried oxide layer which was formed in the annealing limitation which was performed on the wafer after the oxygen implanting limitation, which while on clearly been performed on "said wafer" instead of the substrate, does have limitations at least attempting to related to the porous region that would contradict the liver requirement. From review of the specification, it appears that this limitation & that of new claim 27 are probably intended to be derived from teachings of [0043], however the unclear association of limitations creates significant problems & confusion as written. Would phrasing such as -- wherein after said annealing portions of said porous silicon containing region located beneath said uniform buried oxide layer now contain voids --, provide applicants intended meaning? See an analogous phrasing or language problems in **claims 31 & 36**, however claim 31 is further complicated by the required "plurality of uniform... regions", while claim 36 which includes language as in claim 27 is clearer (except when there is more than one buried oxide region = layer), but it still appears to reference to the entire initial porous region, when probably only a portion thereof was intended.

Also in **claim 26**, lines 12-13 introduce "a semiconductor-on-insulator (SOI) wafer, which provides a contradictory definition to the preambles limitation of "a silicon-on-insulator (SOI) substrate", it and creates another uncertainty by introducing a third potential workpiece, without a clear relationship to the previous "said wafer" or "a Si-containing substrate", as the newly introduced wafer on which the uniform buried oxide layer is claimed to be formed by precipitation of oxides has no antecedence to either "said wafer" or "a Si-containing substrate". Furthermore, given that the preamble is directed to fabricating a **silicon**-on insulator substrate, given that the claimed epitaxial deposition is not necessarily a silicon layer (only Si-containing), & the "SOI wafer" also does not necessarily have a silicon overlayer,

therefore the preamble is **not commensurate in scope** with the body of the claim. Note that independent **claims 31 & 36** have analogous issues with respect to the preamble not been commenced or in scope with the body the claims, since their toplayer also derives from "a single crystal silicon-containing layer", which is not necessarily a silicon layer per se as defined by the specification.

Independent **claim 31** requires "a **plurality** of **uniform** buried oxide **regions**" (emphasis added), which is required to be interpreted according to applicants' definition provided in their original specification, which means that each of these individual plurality of uniform buried oxide regions must by definition have a **continuous** interface with the overlying Si containing layer (which consequently must be present) & a **continuous** interface with underlying Si-containing substrate, where the thickness variation of the entire region across the entire wafer/substrate **cannot vary** more than 30% of the total thickness of the buried oxide layer. Hence, claim 31 resultant SOI substrate, must by definition have multiple buried oxide layers, each going across the entire substrate, thus essentially stacked from the top towards the bottom of the substrate. It's unclear how applicants' claimed process can do this, since only one porous silicon containing region is formed, the "plurality of patterned oxygen implant regions" all apparently have the same "the oxygen peak" whose description while providing a choice of location, only provides a choice at a single layer position within the wafer/substrate. Therefore, it appears that the plurality & uniform requirements create contradictions that make either the structure or the process impossible to determine or understand how they can occur together. While the examiner may suspect that this lack of clarity is due to applicants providing a definition that is narrower than what they may have desired or intended, this is the definition that was provided in the original specification by applicants, thus must be applied to the claims as written. While providing definitions for relative terms in a specification can be a very desirable thing, any time such a definition is provided care for clarity & context should always be used, since generally we are all stuck with the definition afterwards. **Claim 36** has the option of analogous problems, since "at least one uniform buried oxide region" encompasses both a single

uniform buried oxide region & a plurality of uniform buried oxide regions, with dependent **claim 39** positively requires the "plurality of uniform buried oxide regions".

4. **Claims 26-42** are rejected under 35 U.S.C. **112, first** paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Independent **claims 26, 31 & 36** all require "forming a porous silicon containing region having a porosity of about 0.01 % or greater in an upper portion of a silicon containing substrate", where it is noted that the original independent claims did not have limitations to forming the poorest region, but started with the structure already provided, where original claim 7 had the limitation "said porous region of vacancies or voids has a porosity of about 0.01 % or greater", thus original claims only provide support for the existence in a provided structure of a porous region with the claimed porosity range, but not for its formation or its location. In the specification, [0027-33] provide a very specific process performing a porous layer in a Si-containing substrate, by either growing doped Si ingots & using doped wafers cut therefrom, or by ion implanting the silicon containing substrate, then performing electrolytic anodization process as described in these paragraphs, were figure 2A clearly illustrates that the porosity is formed in an upper region of Si-containing substrate 10. No support was found in the specification for the **scope** of this limitation for "forming a porous... region...", which is inclusive of a multitude of processes that may deposit a porous layer of Si-containing semiconductor material, and have absolutely nothing to do with either use of doped material or of electrolytic anodization to cause the porosity, both of which are required by the process as disclosed in the original specification, hence the claims as written clearly encompass a great deal of **New Matter**. It is noted that while dependent **claims 28, 33 & 40** recite use of electrolytic anodization, they do not require the use or presence of any dopant during electrolytic

anodization, hence while the problem is not as severe for these dependent claims, neither is it totally corrected.

Claims 26-42 are rejected under 35 U.S.C. **112, first** paragraph, because the specification, while **being enabling** for forming the claimed porous silicon containing region when using the process as described in [0027-33] requiring both doped Si-containing material & electrolytic anodization thereof, does **not reasonably provide enablement** for forming a porous silicon containing region by means other than electrolytic anodization of a doped silicon-containing substrate or layer, such using virtually any silicon-containing semiconductor deposition process, since almost any deposit of such a process will have a porosity at least within the minimum claimed porosity of 0.01 %, (i.e. a void volume of 1/10,000, or conversely a density of 99.99%, approaching theoretical density). The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to use the invention commensurate in scope with these claims. See immediately preceding paragraph, additionally noting that while the PTO cannot measure the porosity or the corresponding density of materials, very few materials of any type actually approach their theoretical density.

Independent **claims 26, 31 & 36** all have in the third forming limitation a requirement including "forming...oxygen implanted region by **implanting oxygen atoms** into said wafer" (emphasis added), however the original independent claims 1, 22 & 24 all required "implanting oxygen ions...", while the implanting steps discussed in [0037-42] & [0049] are all directed to oxygen ion implantation, and while the broader oxygen atom implanting of the present claims, is inclusive of ion implantation of oxygen, no support is found for atomic implantation of oxygen in the scope claimed, which is inclusive of implanting neutral atoms or even uncharged oxygen molecules to form the oxygen implantation region. It is noted that while the specification may sometimes referred to "oxygen implant step", this is only considered a shorthand notation referring back to the beginning of the discussion on this step, which clearly requires oxygen ions to be implanted. Therefore, the claim limitation to "implanting oxygen atoms" is considered

to encompass **New Matter**, not supported or enabled by the original specification. Also note with respect to new **claim 30, 35 & 42**, that while original independent claims have support for the buried oxide layer having a thickness of 0-100 nm (i.e. nonexistent up to 100 nm), it is only for when **ion** implantation has been employed using oxygen doses of 1 E17 atom/cm^2 or less, noting that the use of "atoms" in the units does not negate the fact that it is already required for the atoms to be oxygen ions. Therefore, these dependent claims may also be considered to encompass **New Matter**, especially considering the thickness disclosure in the specification with respect to the buried oxide layer teaches 10-1000 nm or about 20-500 nm in [0045], or 5-100 nm or 10-80 nm in [0050], where the latter teachings of [0050] would appear to be particularly relevant as presently claim processes explicitly deposit a silicon containing layer over the poorest region.

Claims 26-42 are rejected under 35 U.S.C. **112, first** paragraph, because the specification, while being **enabling for** oxygen **ion** implantation into the porous silicon region, does **not reasonably provide enablement** for oxygen **atom** implantation into the porous silicon region. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to use the invention commensurate in scope with these claims. See immediately preceding paragraph, additionally noting techniques and means for implanting atoms that are not ions into a substrate, are significantly different than ion implantation techniques, and reasonably expected to produce different structural effects, such that no clear enablement for use in this process of atomic implantation to produce the very specific effect of ultimately forming SOI structure in the substrate, which is the result of the taught series of steps.

Independent **claims 31 & 36**, due to applicant's definition of "uniform" in [0012] which defines "uniform buried oxide" layer or region either require positively or in the alternative, plural uniform buried oxide layers, which as discussed above in section 3 must be uniform across the entire wafer/substrate, thus as necessitated by applicant's specification that definition must be over one another, however the

only actual plural buried oxide layers disclosed in the specification as illustrated in figure 2D or 2F are discontinuous & on the same level in a layer in the substrate, where ref #18 illustrated in figures 2E-2H may mean either "uniform buried oxide layer" or "buried oxide region" ([0043]), thus the requirements of claims 31 & 36, plus their dependent claims, read in light of the specification's definition of "uniform", are not supported by the original specification, thus constitute **New Matter**. Note that this particular problem could be removed by removing the "uniform" requirement.

Claim 31-42 are rejected under 35 U.S.C. **112, first** paragraph, because the specification, while being **enabling for** forming a single **uniform** buried oxide layer (or region) via the taught process **or** plural buried oxide regions all on the same level or layer in a substrate, does not reasonably provide enablement for forming two or more **uniform** buried oxide layers (or regions) via the taught process, which by definition must be different layers or levels in the substrate. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to use the invention commensurate in scope with these claims. See paragraph immediately above.

5. **Claim 38** is objected to under 37 CFR 1.75(c), as being of **improper dependent** form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

While the examiner very much appreciates when a relative term is clearly defined at the claims, including when it is also defined specification, when the latter occurs that definition needs to be in the same claim were the relative term is introduced, otherwise the dependent claim that provides the definition already present in the specification, does not further limit the preceding limitation. Furthermore, it actually causes confusion & uncertainty, as it implies that the relative term initially introduced without the definition, has some broader undefined meaning than in the definition required by the specification.

6. Applicant's amendments (i.e. new claims) have removed previous prior art rejections of the 3/17/2009 action, nor does it appear that previously considered/reviewed references would read on the presently claimed process, however there are significant clarity, enablement & support issues outstanding, hence further consideration of patentability will depend on how & if applicants amend their claims to overcome both the 112, first & second rejections above, and dependent on updating of the search, plus any further search necessitated by any changes made in the claims, providing no applicable references are found on such an update/further search.

7. **Applicant's arguments** filed 6/1/2009 & discussed above have been fully considered but they are not persuasive due to the new problems introduced into the new set of claims.

Applicant's arguments with respect to claims 26-42 have been considered but are moot in view of the new ground(s) of rejection.

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. **Any inquiry** concerning this communication or earlier communications from the examiner should be directed to **Marianne L. Padgett** whose telephone number is **(571) 272-1425**. The examiner can normally be reached on M-F from about 9:00 a.m. to 5:00 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Meeks, can be reached at (571) 272-1423. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Marianne L. Padgett/
Primary Examiner, Art Unit 1792

MLP/dictation software

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